CS 681-01 Digital Design

Sequential Logic

Lab 06 Testing

Goal N-bit Register

SR Latch

↓

Clock

↓

D Latch

↓

D Latch with CLR

↓

Multiplexors

↓

D flip-flop

↓

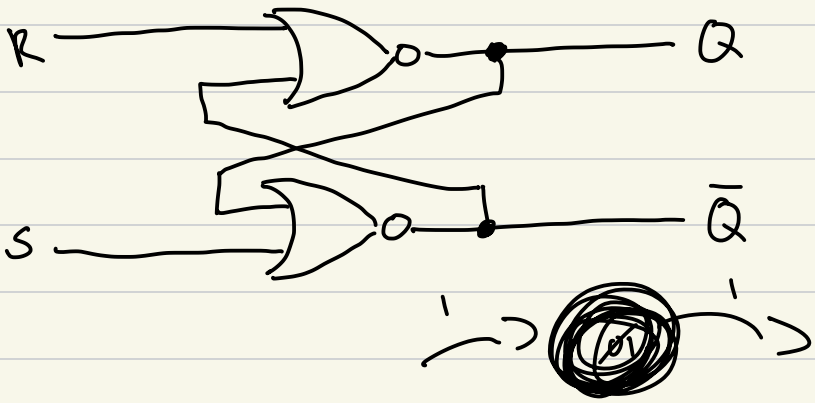
D flip-flop CLR EN → 1 bit Register

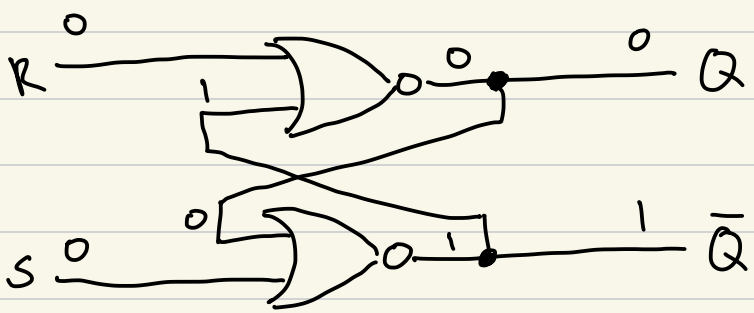
↓

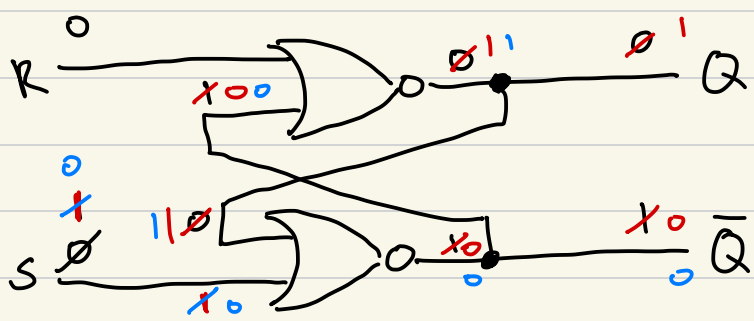
N-bit Register

Static RAM

SR Latch Set Reset

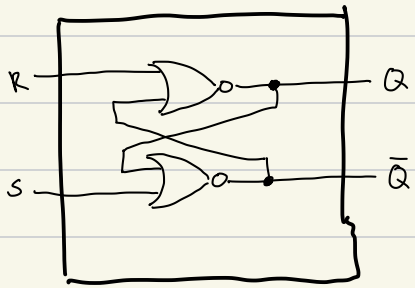




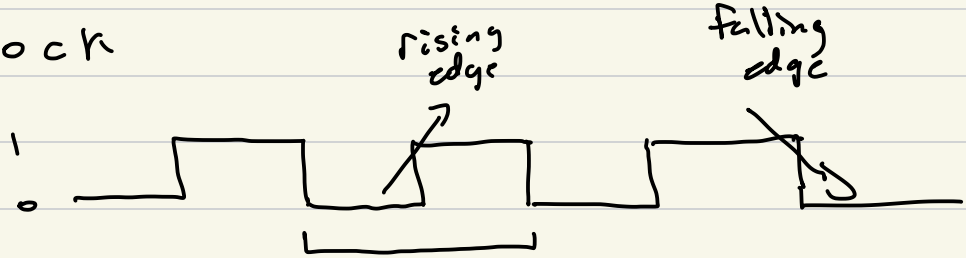


R S	Q $\bar{Q}$
0 0	0 1
0 1	1 0
0 0	1 0
1 0	0 1
0 0	0 1
1 1	X X

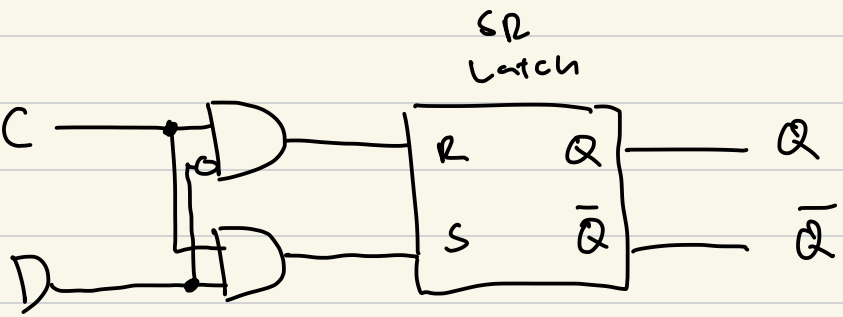
SR Latch



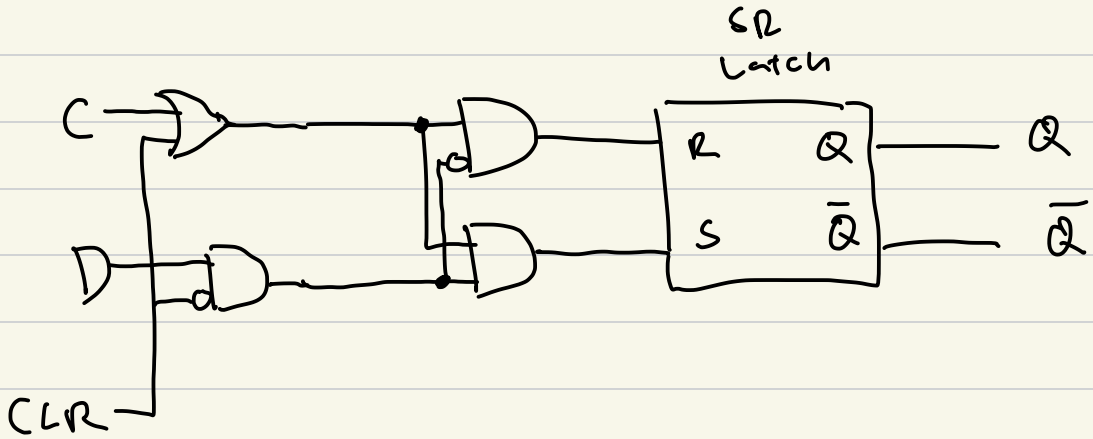
Clock



D Latch

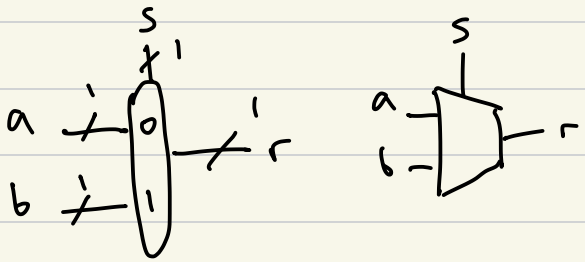


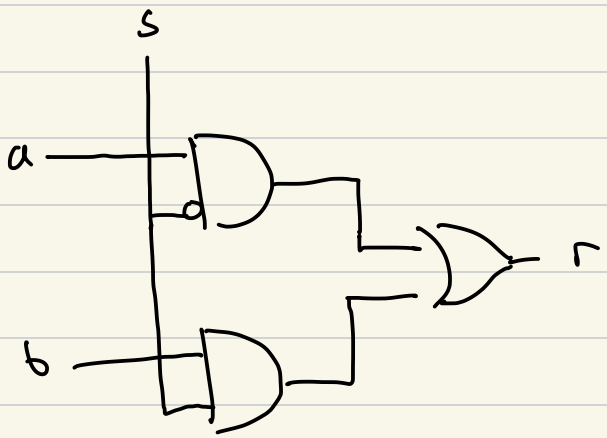
D Latch with CLR

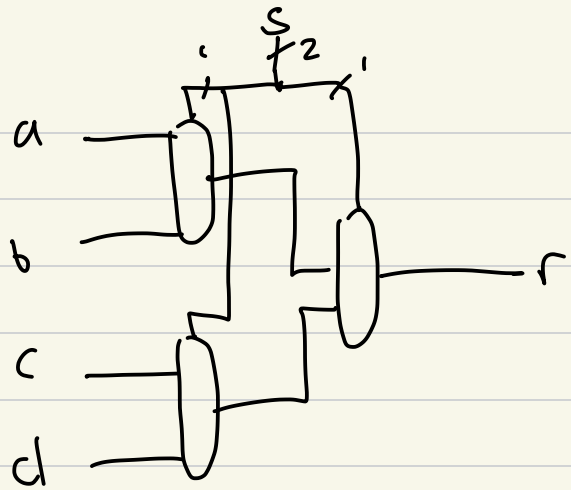


Multiplexor

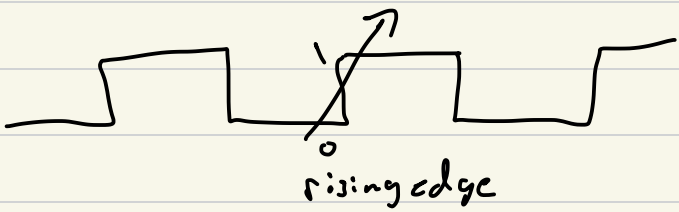
a	b	s	r
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

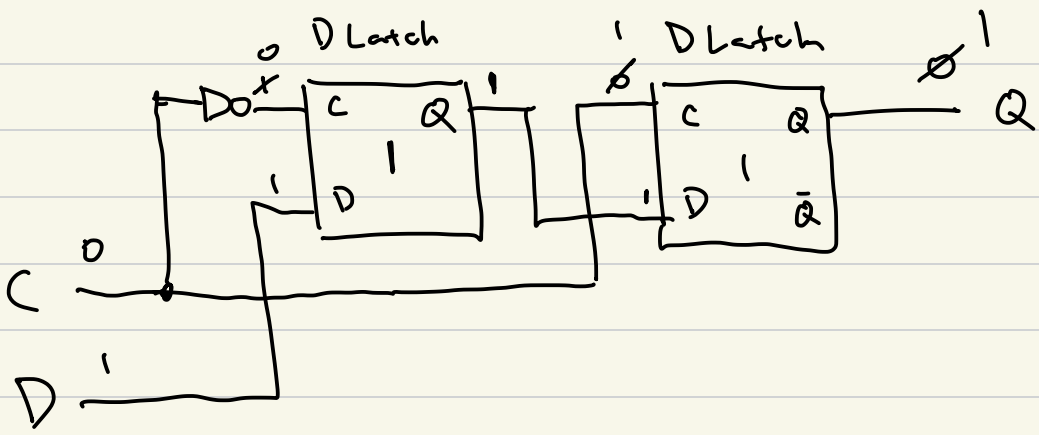






D flip-flop rising edge





D flip-flop with CLR and EN